Webinar Chips Joint Undertaking and calls for proposals in 2024

15 March 2024

VINNOVA

Agenda

1. The EU partnership program Chips JU, Anton Chichkov (Chips JU office).
2. ECS Strategic Research and Innovation Agenda 2024 (ECS-SRIA 2024), Paolo Azzoni (Inside association).
3. Break (15 min)
4. Call 2024 with South Korea (Jeannette Spühler & Maia Kim)
5. Chips JU Calls 2024, Vinnova
   - Calls 2024 IA, RIA (Adela Saavedra Granholm & Sverker Brundin)
   - Other relevant calls (Sverker Brundin)
6. Q & A session

Arbetsgrupp på Vinnova–Chips JU

Adela Saavedra Granholm
INSATSANSVARIG

DELEGAT I PAB OCH GB

Lars Gustafsson

DELEGAT I PAB OCH GB

Sverker Brundin

DELEGAT I PAB OCH GB

Jeannette Spühler

NATIONAL CONTACT POINT (NCP)

HORIZON EUROPE, CLUSTER 4

PAB: Public Authorities Board.
GB: Governing Board.

VINNOVA

The EU partnership program Chips Joint Undertaking

Anton Chichkov (Chips JU office)

VINNOVA

CHIPS JOINT UNDERTAKING

Anton Chichkov

March 15, 2024

EUROPEAN PARTNERSHIP

What is Chips Joint Undertaking?

Public-private partnership (PPP)

Partnerships between public authorities and industry intend to bring project results closer to the market and improve the link between research and societal growth. The PPPs are based on long term contracts that can take many different legal forms, from contractual partnerships to specific legal entities.

Joint undertaking (JU)

A Joint Undertaking is an institutionalized PPP with its own legal identity, with its own governance, budget etc.. The JUs are established by an EU regulation.

Chips JU

Chips JU was established in September 2023, in an amendment to the Single Basic Act to implement the first pillar of the Chips Act and to continue the activities of its predecessors in the field of electronic components and systems (ECS). The Chips JU is a tri-partite partnership between the EC, the participating states and European industries; most of our actions are funded jointly and equally by these actors.

Chips Act: Entry into force, 21 September 2023

Signatures 13 September, Publication 18 September 2023

Roberta Metsola (European Parliament President)

José Manuel Albares Bueno (Council Presidency)

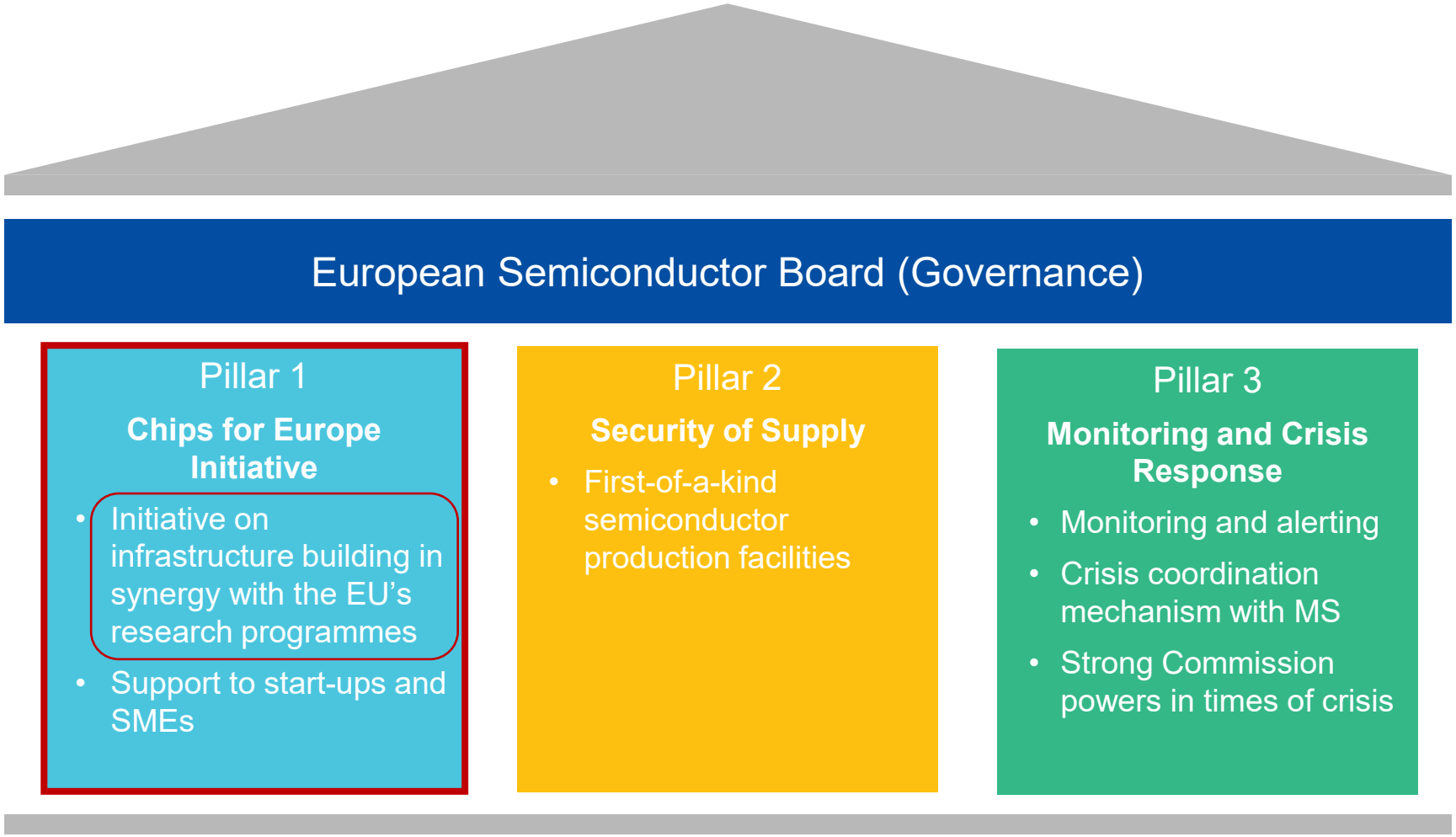
Chips Act:

https://eur-lex.europa.eu/eli/reg/2023/1781/oj

Single Basic Act amendment:

https://eur-lex.europa.eu/eli/reg/2023/1782/oj

THE 3 PILLARS OF THE CHIPS ACT



CHIPS JU AND ITS PREDECESSOR KEY DIGITAL TECHNOLOGIES JU (KDT JU)

Non-Initiative

- **KDT General Objectives**
  - a) Reinforce EU strategic autonomy in electronic components and systems
  - b) Establish EU scientific excellence and innovation leadership
  - c) Ensure that components and systems technologies address Europe's societal and environmental challenges

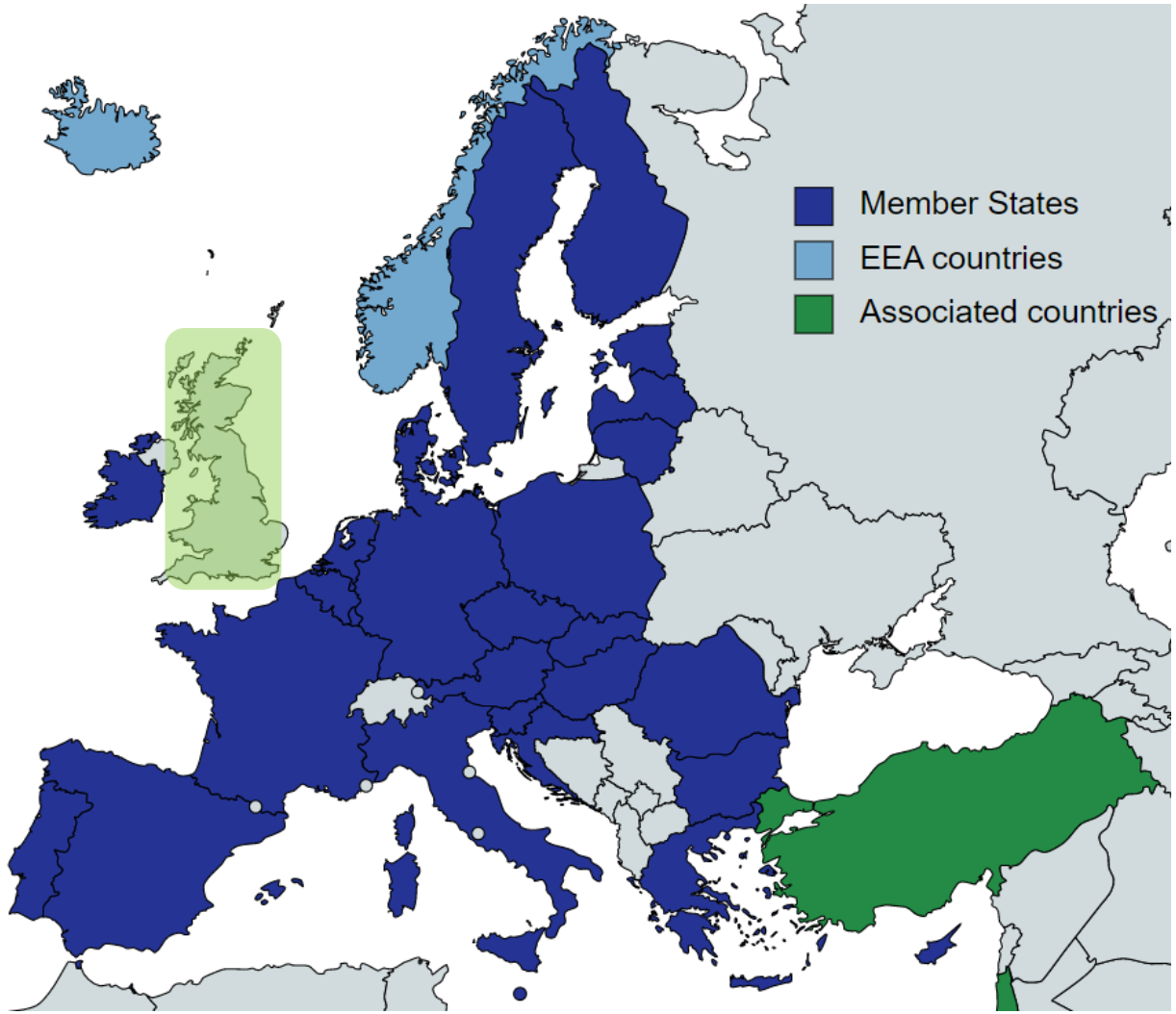
Initiative

- **From KDT to Chips JU**
  - d) Pilot lines
  - e) Design platform
  - f) Competence centers
  - g) Quantum chips technology

  Digital Europe Programme in addition to Horizon Europe

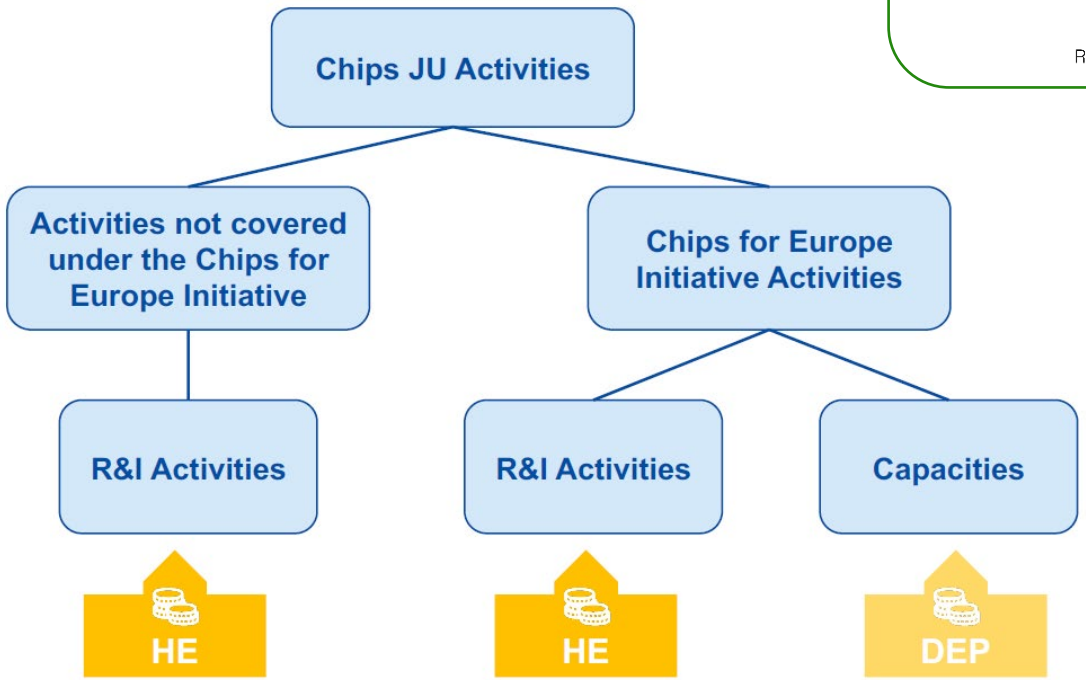
- **Disclaimed:** ***we know that the WP2023-2027 will need to be updated/amended in the spring and some details on the following pages may change:***

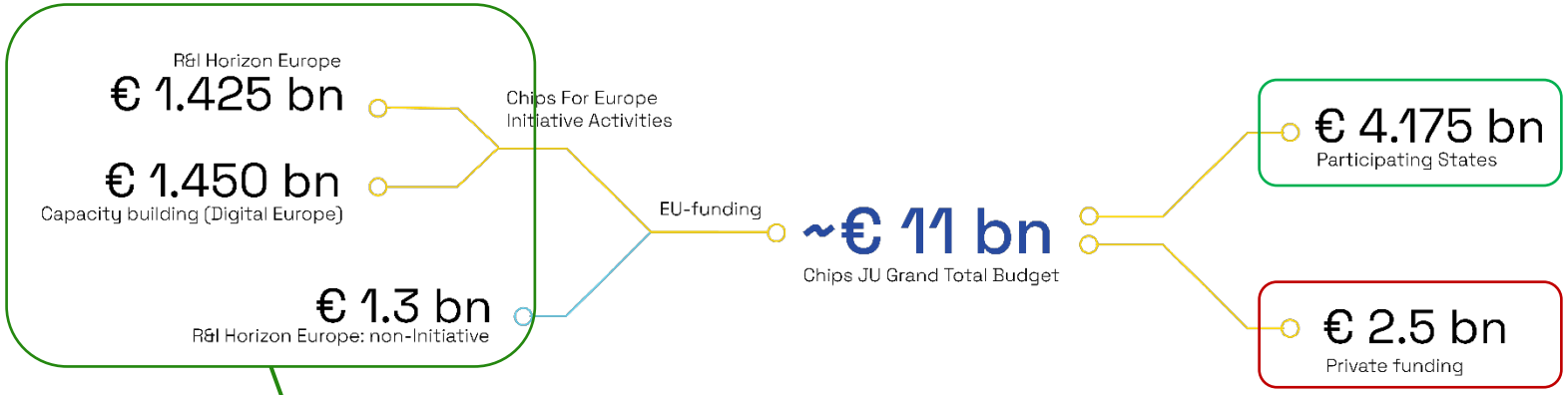
https://www.chips-ju.europa.eu/Library/



EUROPEAN PARTNERSHIP

CHIPS JU





EU Contribution to Chips JU (excl	Chips for Europe Initiative	Non-Initiative	Total
R&I (Horizon Europe)	1.425	1.300	2.725
Cap building (DEP)	1.450	n.a.	1.450
Total	2.875	1.300	4.175

CHIPS JU NON INITIATIVE CALLS

Anton Chichkov

March 15, 2024

EUROPEAN PARTNERSHIP

CHIPS JU NON-INITIATIVE CALLS 2024

Action	Title	Maximum JU Funding (M€)
HORIZON-Chips 2024-1-IA-T1	Global IA call according to SRIA 2024	103.00
HORIZON-Chips 2024-1-IA-T2	Focus topic on “High Performance RISC-V Automotive Processors supporting SDV”	20.00
HORIZON-Chips 2024-1-IA-T3	Focus topic on “Service Oriented Framework for the Software Defined Vehicle of the future"	20.00
HORIZON- Chips 2024-2-RIA-T1	Global RIA call according to SRIA 2023	52.00
HORIZON- Chips 2024-2-RIA-T2	Focus topic on “Sustainable and greener manufacturing”	15.00
HORIZON- Chips 2024-3-RIA	Joint call with Korea on Heterogeneous integration and neuromorphic computing technologies for future semiconductor components and systems	6.00
		216.00

Chips JU IA proposals

An IA proposal is characterized by:

- The activities have their centre of gravity at the **TRL 5-8.**
- Execution by **an industry led consortium**
- Developing **innovative technologies and/or using them in innovative ways**
- Establishment of a new and realistic innovation environment **connected with an industrial environment,** such as:
  - a pilot line facility capable of manufacturing
  - a zone of full-scale testing
  - a development of new processes or tools and their introduction in several domains
  - the development of frameworks or platforms together with the usage of these frameworks or platforms in innovative products.
- IA Prjects should contribute to, short to midterm **economic value creation** in Europe

Focus topic on High Performance RISC-V Automotive Processors Supporting SDV

- RISC-V still requires important extensions and add-ons in order to support *high-performance automotive quality processing* needs.
  - Efforts should be focussed on the development of an **automotive RISC-V reference hardware platform**.
  - **Open-source RISC-V based hardware** system implementation of the **SDV Hardware Layer** compatible with one or multiple widely-agreed-upon **Hardware Abstraction Layers** of the vehicle of the future is targeted.
  - The expected RISC-V reference platform shall be targeted for **commercial use** and should comply with **industry standards** especially with respect to quality and safety.
  - It should contain all assets needed to enable the adoption of RISC-V cores throughout the European automotive ecosystem.

Focus topic on Software-define vehicle middleware and API framework for the vehicle of the future

- Europe needs to join forces in order to lead on the Software Defined Vehicle (SDV) technology
- The SDV software stack should be extended by a **Middleware and Application Programming Interface (API) Framework**
  - **To** supports different technologies.
  - This framework should expose the hardware functionalities directly as APIs or services
  - This car OS should be independent, standardized & interoperable, as well as safe, secure, efficient and easily accessible
- This call has a focus on
  - ***Modular (open-source)*** *building blocks*
  - ***Open architectures*** of the ***SDV middleware and API framework*** for the *vehicle of the future*.
  - ***Holistic engineering framework***

Chips JU RIA proposals

- RIA proposal is characterized by
  - The activities have their centre of gravity at **TRL 3-4**
  - Execution normally by an **academy led consortium**
  - Developing **innovative disruptive technologies**
  - Targeting **demonstration of the innovative approach**, clearly addressing relevant societal challenges
  - Demonstrating **value and potential in a realistic lab environment** reproducing the targeted application
  - Having a **deployment plan showing the valorisation for the ECS ecosystem** and the contribution to the Chips JU goals and objectives

Focus Topic Sustainable and Greener Manufacturing

- This focus topic concerns the development of a **sustainable and greener semiconductor manufacturing** through the reduction of its environmental footprint with a **focus on materials**. The results of the project are expected to contribute to the following outcomes:
  - Increase the use of **environmentally friendly materials**, chemicals and solvents.
  - **Minimization of waste** and emissions during production and processing
  - Prevention of a future scarcity of some critical materials for SC processing through a **more efficient and cost-effective products** and **electronic waste recycling** in process., including chips and PCBs.

Joint call with Korea

- This joint call for proposals between the Republic of Korea and the EU addresses the topics related to **Heterogeneous integration and neuromorphic computing technologies** for future semiconductor components and systems and intends to set a framework
  - To strengthen the relation between R&I players in both jurisdictions
  - To undertake joint R&I for EU and Korean R&I teams by cooperating in pre-competitive projects on areas which are in the interest of both jurisdictions.
  - To build trust for further cooperation.
- This joint call topic will be co-funded by South Korea (KR) and the European Union (EU)
- This call has very specific conditions. Please conslut the call text in the work programme

EU Funding Rates

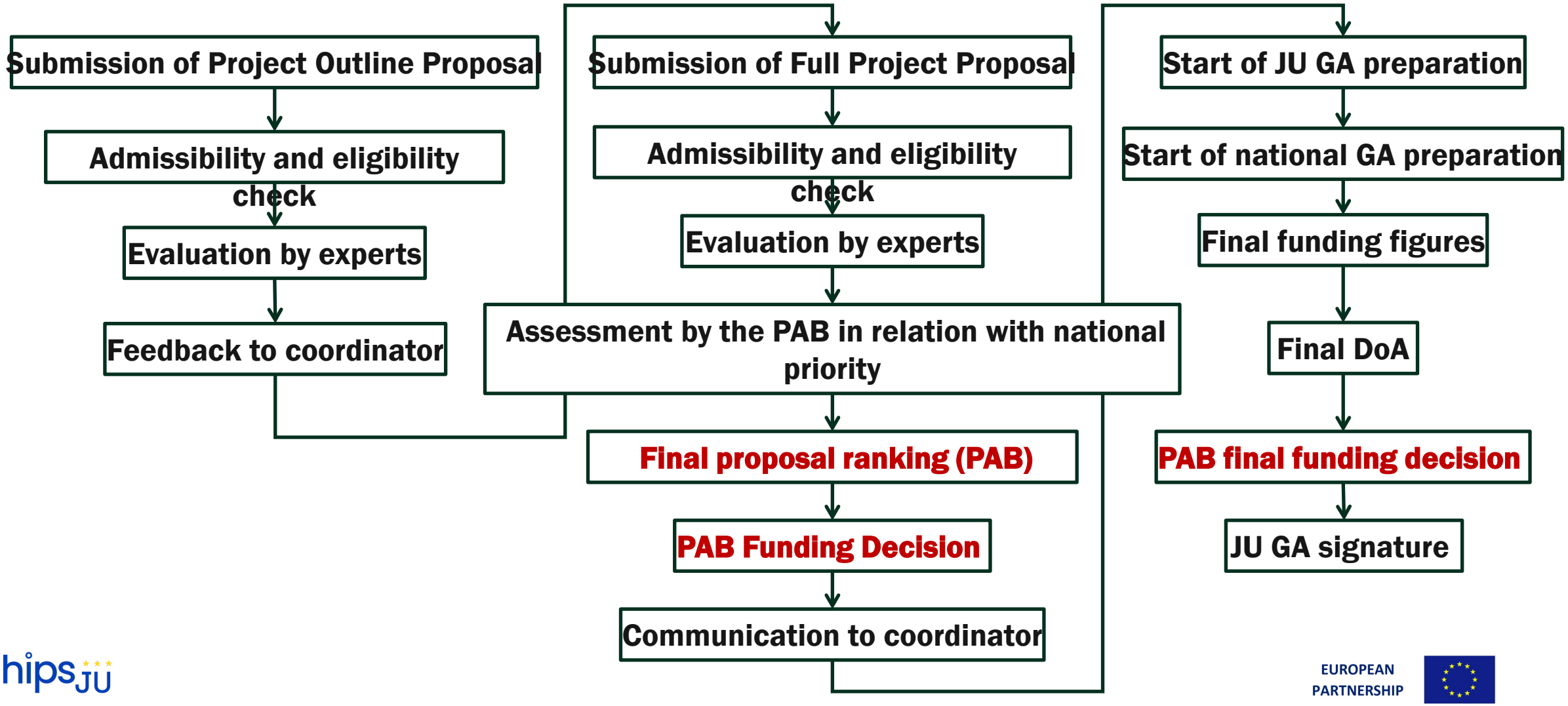
Type of beneficiary	2024-1-IA	2024-1-IA Focus Topics	2024-2-RIA	2024-2-RIA Focus Topic	2024-3-IA
Large Enterprise	20 %	25 %	25 %	25 %	100%
SME	30 %	30 %	35 %	35 %	100%
University/Other (not for profit)	35 %	35 %	35 %	35 %	100%
National Funding	YES	YES	YES	YES	NO

Schedule

Calls 2024-1 and 2024-2	Two stage Call with submission of Project Outline (PO) and Full Proposal (FPP)
Publication date	06 February 2024
Deadline PO Phase	14 May 2024 at 17:00 Brussels Time
Deadline FPP Phase	17 September 2024 at 17:00 Brussels Time
PAB selection	November 2024
Grant preparation	December 2024 to April 2025
Start of the projects	around May 2025

For the Call2024-3, there is no PO phase only an FPP phase with e deadline on 14 May 2024

Proposal Evaluation, Selection, and Grant Agreement Preparation



Useful links

Check regularly the call information under the CHIPS website:

https://www.chips-ju.europa.eu/

Address eventual questions related to the calls to:

calls@chips-ju.europa.eu

Consult the sections on the 2024 calls in the:

Chips JU Work Programme

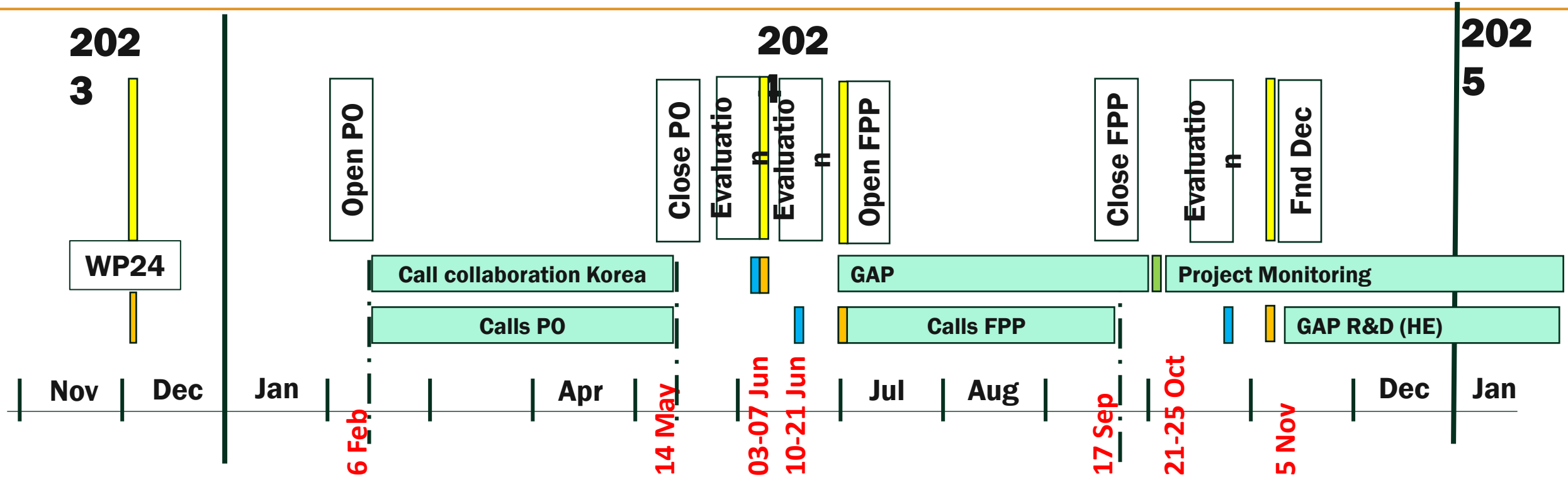
Chips JU Calls Planning

Anton Chichkov

March 15 2024

EUROPEAN PARTNERSHIP

PLANNING CALLS 2024 NON-INITIATIVE



Chips JU Calls 2024

Vinnova

VINNOVA

HORIZON- Chips 2024-3-RIA Joint call with South Korea

Jeannette Spühler (Vinnova)
Maia Kim (EU-Korea Research Centre)

VINNOVA

Call HORIZON-JU-Chips-2024-3-RIA: Joint call with Korea on Heterogeneous integration and neuromorphic computing technologies for future semiconductor components and systems

- New materials, process, device, integration and design concepts for neuromorphic computing systems supporting very low energy consumption, connectivity and embedded functions for mobile applications.
- Alternative manufacturing process technologies for semiconductor chips including frontend or backend for heterogenous integration.
- Advanced packaging solutions aiming at heterogeneous integration of multiple functions and materials for applications in AI, communication (RF, mmW or THz), sensing, actuating, power management and active/passive device integration.

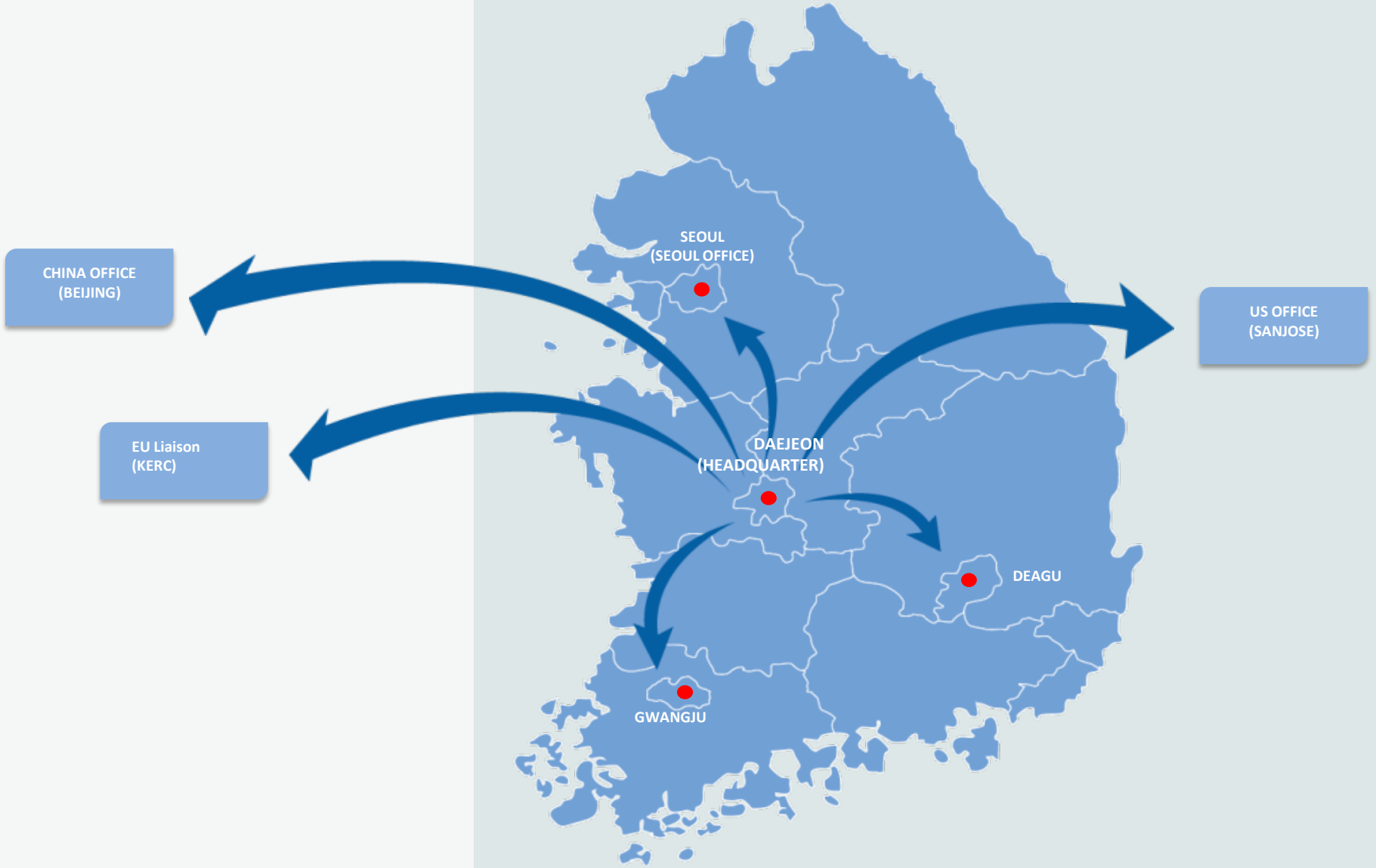
Call HORIZON-Chips-2024-3-RIA: Joint call with Korea on Heterogeneous integration and neuromorphic computing technologies for future semiconductor components and systems

- Type of Action: RIA (TRL 2-4),
- Total EU-Budget: 6 MEURO (~1,5 MEURO/project), RoK approximately the equal amount
- Typical duration: 3 years
- Deadline: 14th May 2024
- For EU proposal, rules of Horizon Europe apply
  - Consortium: EU Horizon Europe consortium and KR consortium
  - EU partners receive EU Funding from Chips JU (NO NATIONAL BUDGET!), KR partners from NRF
  - EU Contribution as % of the eligible cost: 100 % (for Large enterprise, SME, University)

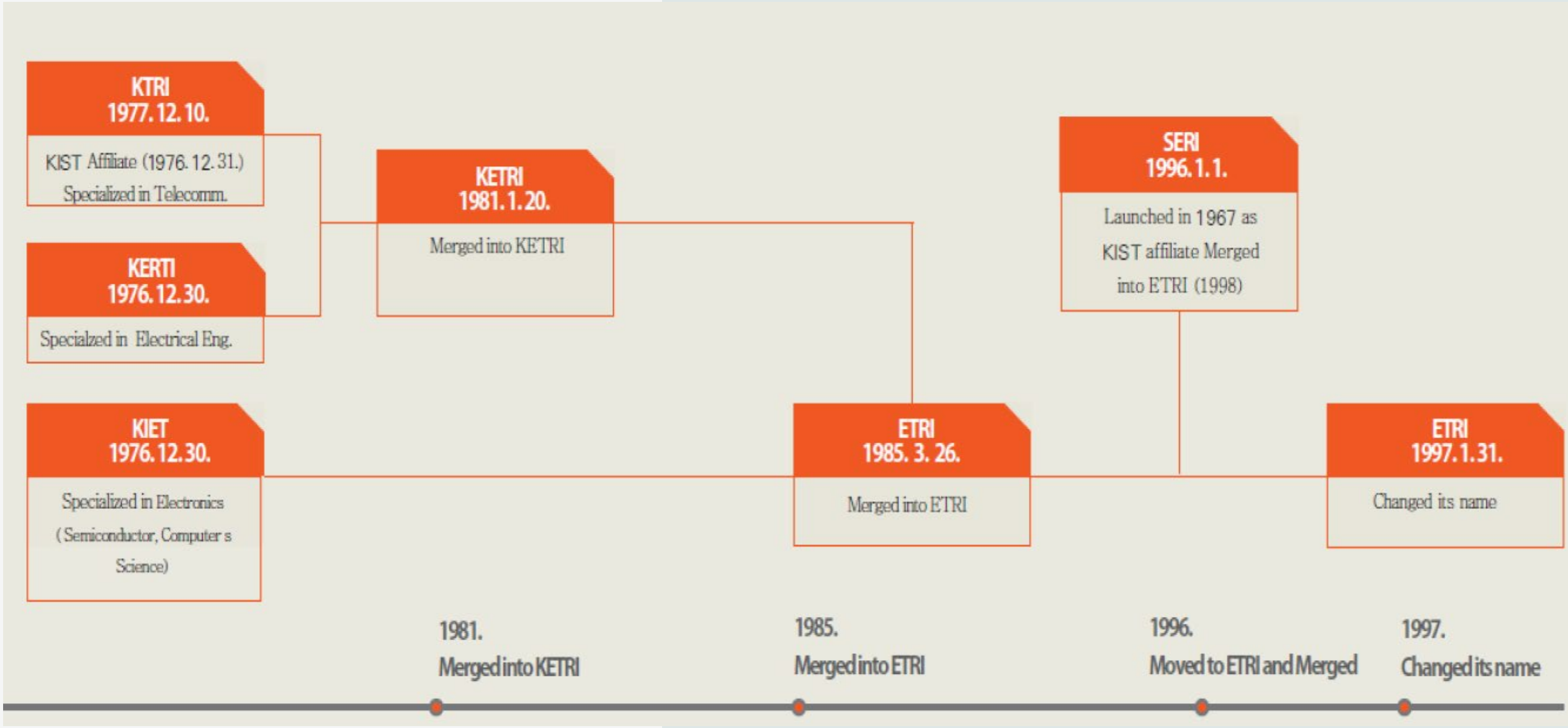
ETRI

Electronics and Telecommunications
Research Institute

where we are

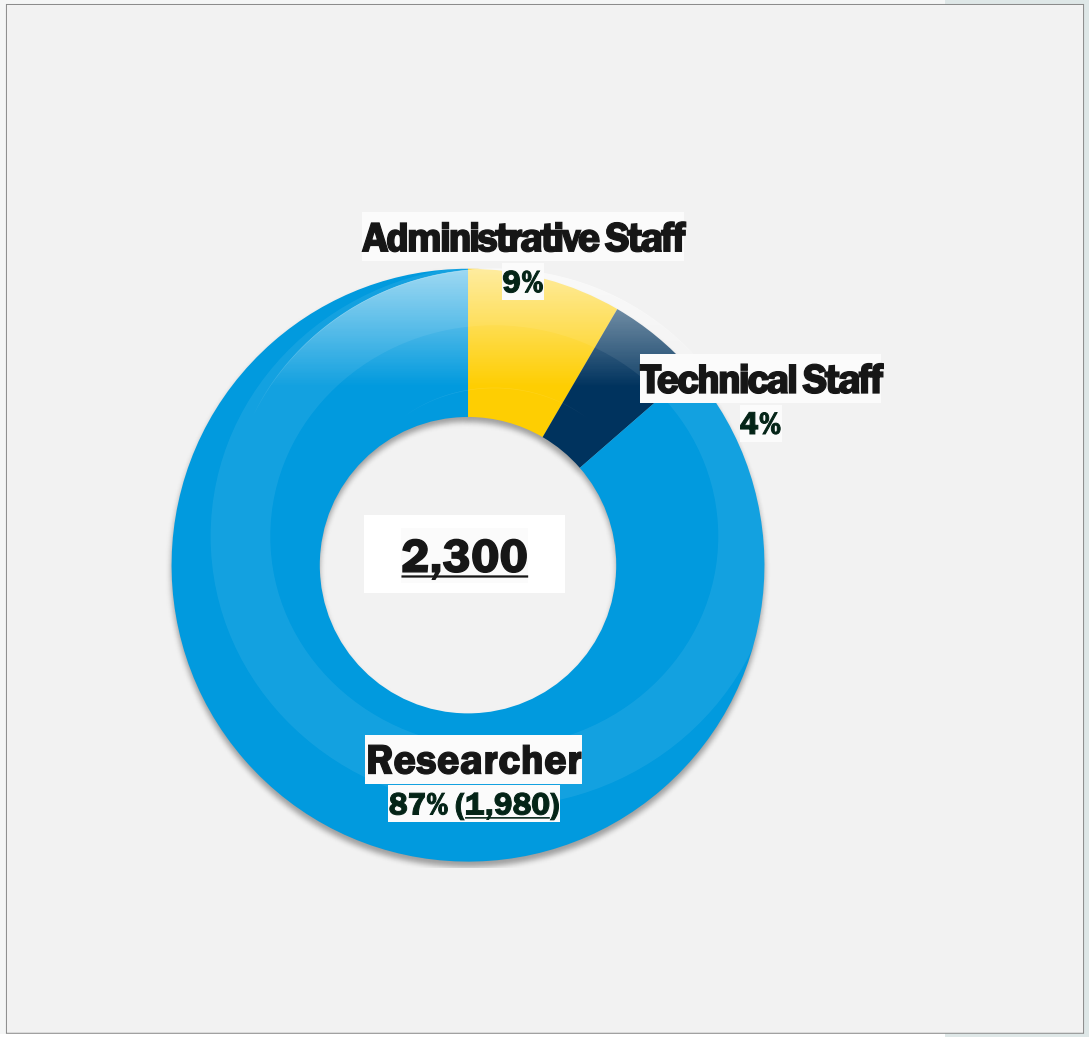

CHINA OFFICE
(BEIJING)
EU Liaison
(KERC)
SEOUL
(SEOUL OFFICE)
DAEJEON
(HEADQUARTER)
DEAGU
GWANGJU
US OFFICE
(SANJOSE)

History

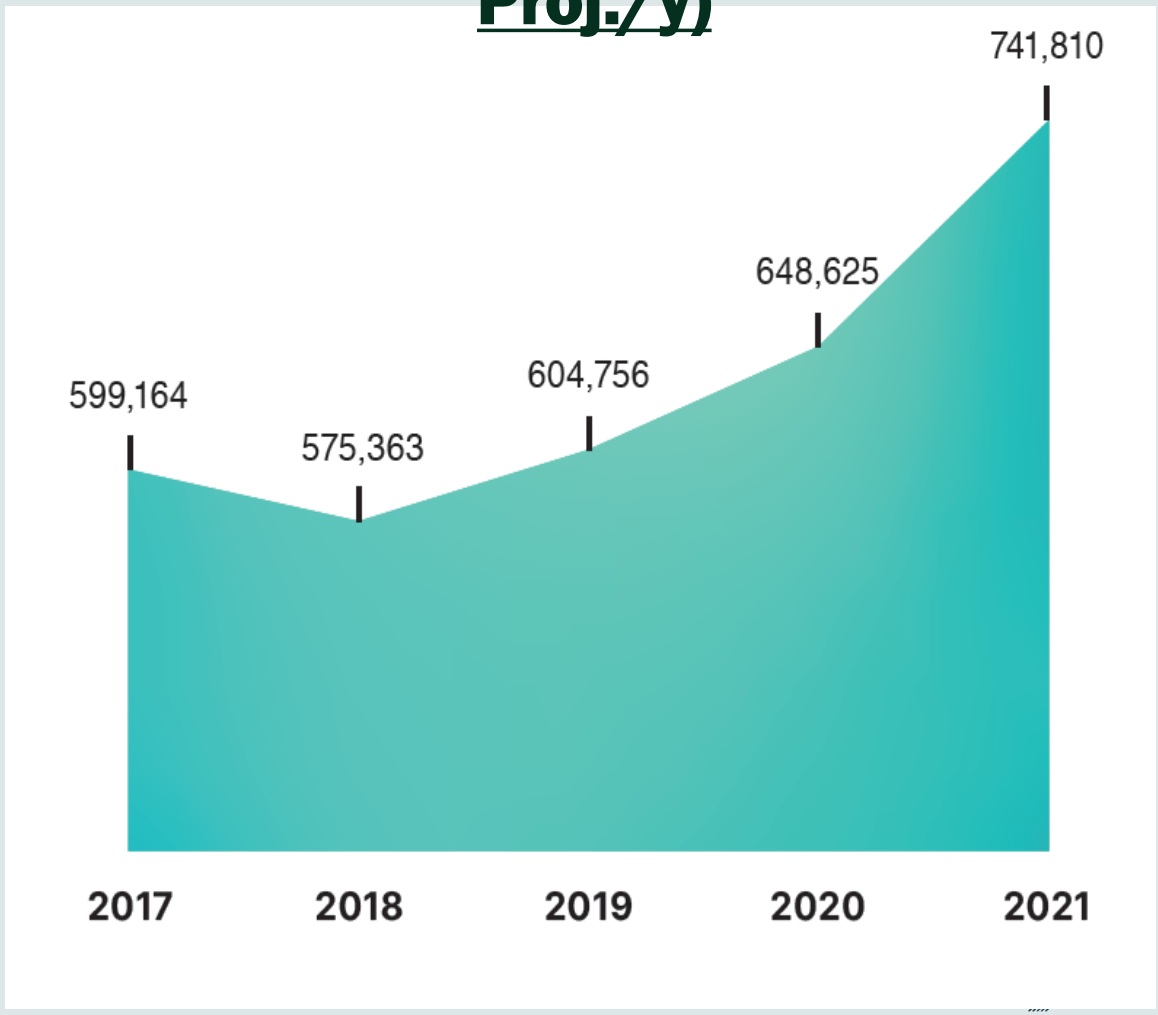

KTRI
1977. 12. 10.
KIST Affiliate (1976. 12. 31.)
Specialized in Telecomm.
KERTI
1976. 12. 30.
Specialzed in Electrical Eng.
KIET
1976. 12. 30.
Specialized in Electronics
(Semiconductor, Computer s
Science)
KETRI
1981. 1. 20.
Merged into KETRI
ETRI
1985. 3. 26.
Merged into ETRI
SERI
1996. 1. 1.
Launched in 1967 as
KIST affiliate Merged
into ETRI (1998)
ETRI
1997. 1. 31.
Changed its name
1981.
Merged into KETRI
1985.
Merged into ETRI
1996.
Moved to ETRI and Merged
1997.
Changed its name

People & Projects

People: 2,300



$ 600 mil. (600 Proj./y)



Research Org.

https://www.etri.re.kr/eng/sub6/sub6_01020102.etri?departCode=131&departInfoC

Artificial Intelligence, Computing

- Div. Future Computing Research
- Div. AI SoC Research
- Div. Cyber Security Research
- Div. Quantum Technology Research

Superintelligence

- Div. Intelligence Information Research
- Div. Mobility Robot Research
- Div. Creative & Basic Technology Research
- Div. Materials and Components Research

Hyper-Reality Metaverse

- Div. Media Research
- Div. Content Research
- Div. Reality Devices Research

Telecommunications

- Mobile Communication Research
- Network Research
- Radio Research
- Satellite Communication Research
- Photonic/Wireless Devices Research

Digital Convergence

- Div. Air Mobility Research
- Div. Industrial Energy Convergence Research
- Div. Digital Biomedical Research
- Div. Defense & Safety Convergence Research

ICT Strategy

- Div. Technology Strategy Research
- Div. Technology Policy Research
- Div. Standards & Open Source Research

Technology Pioneer
Making Happy Future through Digital Innovation

Organization

Audit & Inspection Department

Artificial Intelligence Computing Research Laboratory

Introduction of Research Strategy Laboratory

Introduction of Research & Development Department

Superintelligence Creative Research Laboratory

Terrestrial & Non-Terrestrial Integrated Telecommunications

Introduction of Research

▪ Future Computing Research Division | AI SoC Research Division | ▪ Cyber Security Research Division

▪ Quantum Technology Research Division

AI SoC Research Division

Introduction | Areas for Research & Development

• HW/SW Technology for Hyperscale AI Neural Network Semiconductor(IC)

The ever-growing AI neural networks for achieving near human intelligence require high performance semiconductor IC (Integrated Circuit) design technology and the system development technology which utilizes the IC including the software technology to efficiently operate these systems.

With the experiences in the developments of untra-low power visual AI processing chip and the AB9 chip which is Korea's first developed NPU chip as well as the 5PFLOPS grade AI server (ArtBrain-K) and the accompanying AI-Ware system software, we are developing hyper-scale AI computing semiconductor IC and the AI semiconductor's system SW and platform technology along with hyper-parallel processing core based semiconductor processor for super computer and 64 bit RISC-V core technology for next generation CPU.

TOP

https://www.etri.re.kr/eng/sub6/sub6_01020102.etri?departCode=131&departInfoCode=268

A Policy & Research Bridgehead For Science and Technology Between Korea and the EU

Maia KIM
maia@k-erc.eu
+32 494 93 34 26

Chips JU RIA & IA Calls 2024

Adela Saavedra Granholm (Vinnova)
Sverker Brundin (Vinnova)

VINNOVA

Calls for ‘24

ACTION	TOPIC	ESTIMATED EU EXPENDITURE	VINNOVA'S BUDGET
HORIZON-Chips 2024-1-IA T1	Global call according to SRIA 2024 (IA)	103	3
HORIZON- Chips 2024-1-IA T2	Focus topic on “High Performance RISC-V Automotive Processors supporting SDV”	20	0
HORIZON- Chips 2024-1-IA T3	Focus topic on “Service Oriented Framework for the Software Defined Vehicle of the future”	20	0
HORIZON- Chips 2024-2-RIA-T1	Global call according to SRIA 2023 (RIA)	52	3
HORIZON- Chips 2024-2-RIA T2	Focus topic on “Sustainable and greener manufacturing”	15	0,6
HORIZON- Chips 2024-3-RIA	Joint call with Korea on Heterogeneous integration and neuromorphic computing technologies for future semiconductor components and systems	6	0
	Total	216	6,6

Calls within the Non-Initiative part under Chips JU with financing from the Horizon Europe programme.
IA = Innovation Action
RIA = Research & Innovation Action Currency = EUR

VINNOVA

Where to find the calls

- 1. Vinnova's site: Chips JU Calls 2024-Europeiska samverkansprojekt inom elektroniska komponenter och system (ECS) | Vinnova
- 2. The Chips JU site: Non-Initiative Calls 2024 · Chips Ju (europa.eu)
- 3. The Funders & Tenders portal: Funding & tenders (europa.eu)

Chips JU Calls 2024-European collaborative projects in electronic components and systems (ECS) | Vinnova

VINNOVA

Search In Swedish Log in Menu

Start > Funding > Find funding > Chips JU > Chips JU Calls 2024-European collaborative projects in e...

Chips JU Calls 2024-European collaborative projects in electronic components and systems (ECS)

Closes on 17 September 2024 at 5PM

Chips Joint Undertaking (Chips JU) is an institutionalized partnership program within Horizon Europe, which is funded by the European Commission, funding national authorities in participating countries and participating organisations. Inom Chips JU finances Vinnova collaboration projects with actors along the entire value chain from semiconductor chips and electronic components to systems of systems (SoS), both with a software and hardware focus to contribute to sustainable digital transformation. Areas of application can be mobility, energy, industrial digitalization, digital infrastructure and communication as well as digitalization in agriculture and forestry, health and society.

This web page has been machine translated. If there are any uncertainties, please refer to the Swedish text.

What can you apply for?

For participation in international collaborative projects focusing on electronic components and systems (ECS).

Who can apply?

Swedish companies that meet Vinnova´s eligibility requirements as well as universities and research institutes. Vinnova requires participation from Swedish companies corresponding to at least 60 percent of the total Swedish project budget.

How much can you apply for?

The Swedish consortium can apply for a maximum of EUR 2,000,000 in support from Vinnova for a project. The European Commission can finance the project at the corresponding level. Vinnova´s budget for Calls 2024 is SEK 73 million.

VINNOVA

https://www.chips-ju.europa.eu/applyforfunding/

Chips JU Non Initiative Calls 2024

This page outlines the key steps to follow when applying for funding from the Chips JU Non Initiative Calls 2024.

Read More →

Chips JU Initiative Calls 2023

This page outlines the key steps to follow when applying for funding from the Chips JU Initiative Calls 2023.

Read More →

https://www.chips-ju.europa.eu/noninitiative/

Non-Initiative Calls 2024

Search funding & tenders

Search

Clear all

JU-Chips

Match whole words only

Type

- [x] Grants 6
- [ ] Tenders

Submission status

- [x] Forthcoming
- [x] Open for submission 6
- [ ] Closed

Programming period

6 item(s) found

Programme: Horizon Europe (HORIZON)

HORIZON-JU-Chips-2024-2-RIA Topic 1Global call according to SRIA 2023
HORIZON-JU-Chips-2024-2-RIA-T1 **Call for proposal**
Horizon Europe (HORIZON)

Topic 2 Focus topic on "High Performance RISC-V Automotive Processors supporting SDV"
HORIZON-JU-Chips-2024-1-IA-T2 **Call for proposal**
Horizon Europe (HORIZON)

Topic 2 Focus topic on "Sustainable and greener manufacturing"
HORIZON-JU-Chips-2024-2-RIA-T2 **Call for proposal**
Horizon Europe (HORIZON)

Sweden National Rules - Chips JU Calls 2024

[Chips JU Calls 2024-European collaborative projects in electronic components and systems (ECS) | Vinnova]

What can you apply for?

For participation in international collaborative projects focusing on electronic components and systems (ECS).

Who can apply?

Swedish companies that meet Vinnova´s eligibility requirements as well as universities and research institutes. Vinnova requires participation from Swedish companies corresponding to at least 60 percent of the total Swedish project budget.

How much can you apply for?

The Swedish consortium can apply for a maximum of EUR 2,000,000 in support from Vinnova for a project. The European Commission can finance the project at the corresponding level. Vinnova´s budget for Calls 2024 is SEK 73 million.

VINNOVA

Sweden National Rules - Chips JU Calls 2024

DOCUMENTS:

Vinnova's special conditions Chips JU Calls 2024

Särskilda villkor för deltagande i Chips Joint Undertak... (pdf, 79 kB)

Vinnova's national rules - Sweden National rules Chips JU 2024

Sweden national rules 2024 – Chips JU (pdf, 276 kB)

- National budget Calls 2024: **6,6 millions EUR (73 millions SEK)**
- Maximum Vinnova contribution to one project is limited to **2 000 000 €.**
- The total eligible project costs of participating Swedish companies must amount to at least 60% of the total eligible project costs of all Swedish participants in the project consortium.
- The maximum funding from Vinnova for a single large enterprise, university and research institute is equivalent to **730 000 €.**
- The maximum national funding for a SME is equivalent to **450 000 €.**
- The costs of all partners specified in the project budget shall harmonize with costs in accordance with the Grant Agreement with Chips JU.

VINNOVA

National funding rates

Type of beneficiary	Large Enterprise	SME	University and RTO	Project coordinator: University, RTO	Project coordinator: Company
RIA - Research and Innovation Action	25%	35%	50%	65%	40%
IA - Innovation Action	20%	30%	50%	65%	35%
Focus Topics	25%	35%	50%	65%	35%

- EU commission funding rates: see information in Chips JU Work Programme 2024
- Note: Horizon Europe funding rules determines the eligible costs.
- Additional national funding for Swedish coordination of full project proposal: up to 500 000 SEK, maximum of 80% of eligible costs can be financed.

National rules for participating companies

- Participating companies must be registered as a limited company in Sweden (Aktiebolag).
- Participating companies must have a permanent establishment in Sweden.
- Project activities must be conducted at sites that belong to a participating company.
- Project costs must belong to the participating company.
- Participating companies must be registered for employer's contribution.
- Participating companies must have submitted at least two annual reports to the Swedish Companies Registration Office (Bolagsverket).
- The company’s most recent annual report/ financial statement should show that net sales or equity correspond to at least 50% of the public funding applied for from Vinnova and Chips JU.
- Participating companies must have an annual net turnover of at least 1 million SEK according to the latest annual report.
- Participating companies must have a minimum of three full time employees.

Process Chips JU

CONSTRUCTION OF PROJECT CONSORTIUM

matchmaking-events and ECS collaboration tool.

PROJECT OUTLINE

Project Outline submission to Chips JU 14 May

EVALUATION

International evaluation of Project Outline

FULL PROJECT PROPOSAL

FPP submission to Chips JU 17 September

EVALUATION

International evaluation of FPP.
Vinnova evaluates national relevance in parallel (National Part)

DECISION

Chips JU PAB decision on selected projects for funding 5 December

SUBMISSION OF NATIONAL APPLICATION TO VINNOVA

Submission of short national project application to Vinnova March 2025

VINNOVA

Important dates for Chips JU Calls 2024

6 FEB 2024	14 MAY 2024	17 SEPTEMBER 2024	5 DEC 2024
Opens for application	Last application date project outline (Project Outline) for Calls Chips-2024-1-IA and Chips-2024-2-RIA	Last application date full project application (FPP) for Call Chips-2024-3-RIA	Decision given

VINNOVA

Other relevant calls

For questions, please contact Kontakt för Horisont Europa | Vinnova

Eureka | globalstars-taiwan-2024 (eurekanetwork.org):
With Taiwan.
FROM NOVEMBER 20, 2023 AT 01:00 SWEDEN TIME
TO MAY 21, 2024 AT 17:00 SWEDEN TIME

Eureka | network-projects-quantum-call-2024 (eurekanetwork.org):
With South Korea and France.
FROM FEBRUARY 1, 2024 AT 01:00 SWEDEN TIME
TO MAY 9, 2024 AT 16:00 SWEDEN TIME

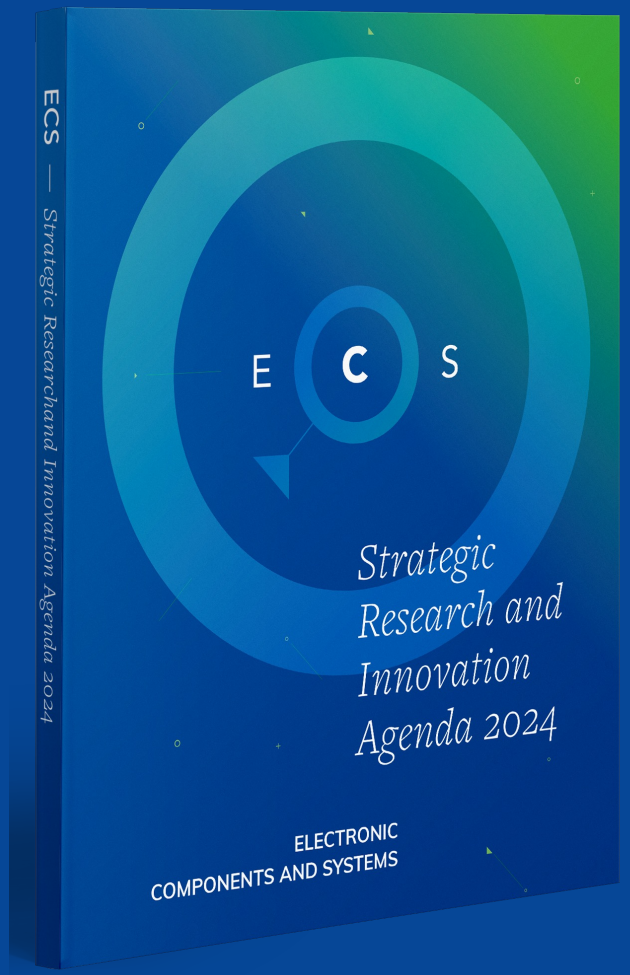
EIC Accelerator Challenges - European Commission (europa.eu)
Enabling the smart edge and quantum technology components
Indicative Budget: EUR 50 million
Aim: To promote the development of novel semiconductor components and integrated smart systems for next-generation edge devices with significant impact.

EIC Pathfinder Challenges - European Commission (europa.eu)
Nanoelectronics for energy-efficient smart edge devices
To explore solutions that will have a drastic impact on decreasing the power consumption of any smart edge device
The proposed solutions should start at TRL 1-2 and reach TRL 3-4

ECS Strategic Research and Innovation Agenda 2024 (ECS-SRIA 2024)

Paolo Azzoni (Inside association)

VINNOVA



ECS SRIA 2024

Webinar Chips JU Calls 2024

Online, 15 March 2024

Paolo Azzoni
Secretary General – INSIDE Industry Association
ECS-SRIA Co-Chair

E C S *Strategic Research and Innovation Agenda 2024*

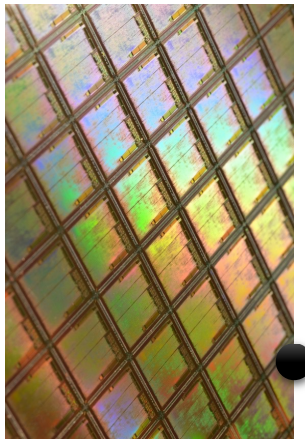
Aeneas

EPoSS. European Association on Smart Systems Integration

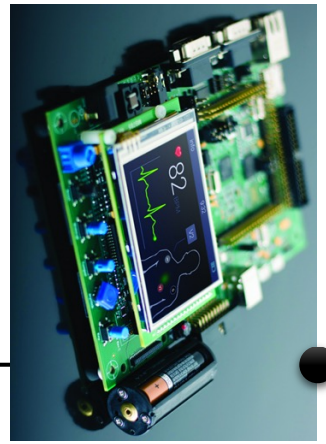
Inside Industry Association

The ECS SRIA - What and Why ?

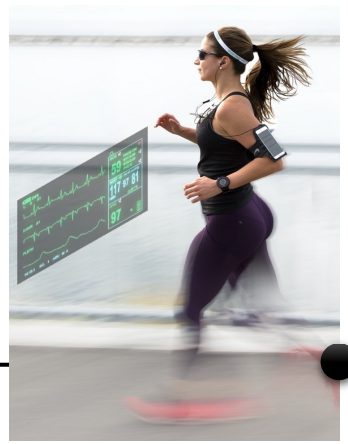
- Collective work of experts across industry, RTO and academia
- Presenting research topics to be investigated over next 15 years
- To foster and accelerate our European digital transformation reflecting European values
- A tool to align and coordinate research policies across Europe
- Covering the whole ECS value chain



Materials, processes, semiconductors, micro & nano electronic components, …



Smart sensors, integrated devices, edge AI, embedded SW, …

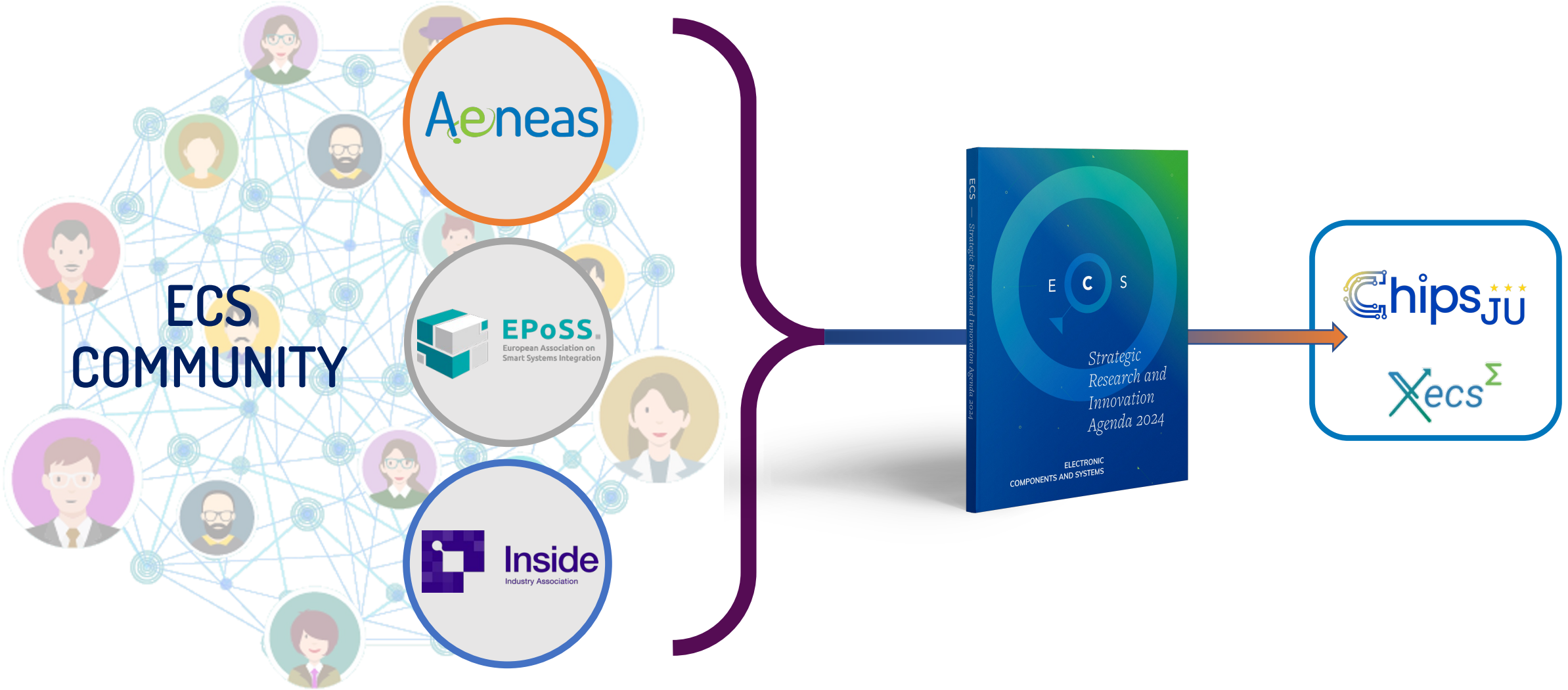


Systems and applications, value creation, societal goals, …

ECS engineering tools

The ECS-SRIA 2024

Basis for the CHIPS JU 2024 Calls for R&I Activities



The ECS SRIA Team 2024

Patrick Cogez
AENEAS
Chairman

Paolo Azzoni
Inside IA
Co-chairman

Nicolas Gouze
EPoSS
Co-chairman

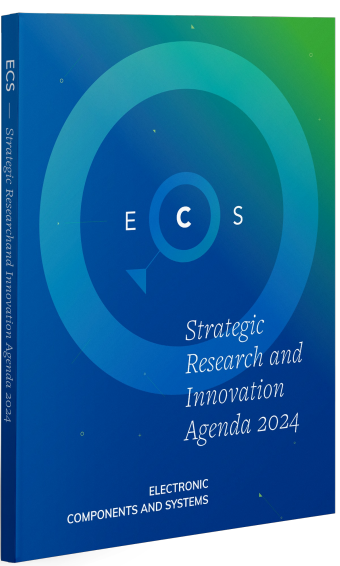
Core Team

- Arco Krijgsman - ASML
- Christophe Wyon - CEA
- Jerker Delsing - LTU
- Jürgen Niehaus - Safetrans
- Patrick Pype - NXP
- Sven Rzepka - Fraunhofer
- Wolfgang Dettmann - Infineon

More than 300 European experts

- Interdisciplinary
- Across the whole ECS value chain
- Representing industry, RTO and academia
- Involved in R&I programmes and standardization activities
- Across almost all participating states

SRIA Synergies in R&I Landscape



Alliance for Internet of Things Innovation

EFFRA
EUROPEAN FACTORIES OF THE FUTURE RESEARCH ASSOCIATION

EuroHPC
Joint Undertaking

6GSNS

BDV
BIG DATA VALUE ASSOCIATION

innovative health initiative

2020 NETWORLD

ECLIPSE FOUNDATION

IRDS
INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS™

2 ZERO

HIR
HETEROGENEOUS INTEGRATION ROADMAP

ERTRAC

PHOTONICS21

QUIC
European Quantum Industry Consortium

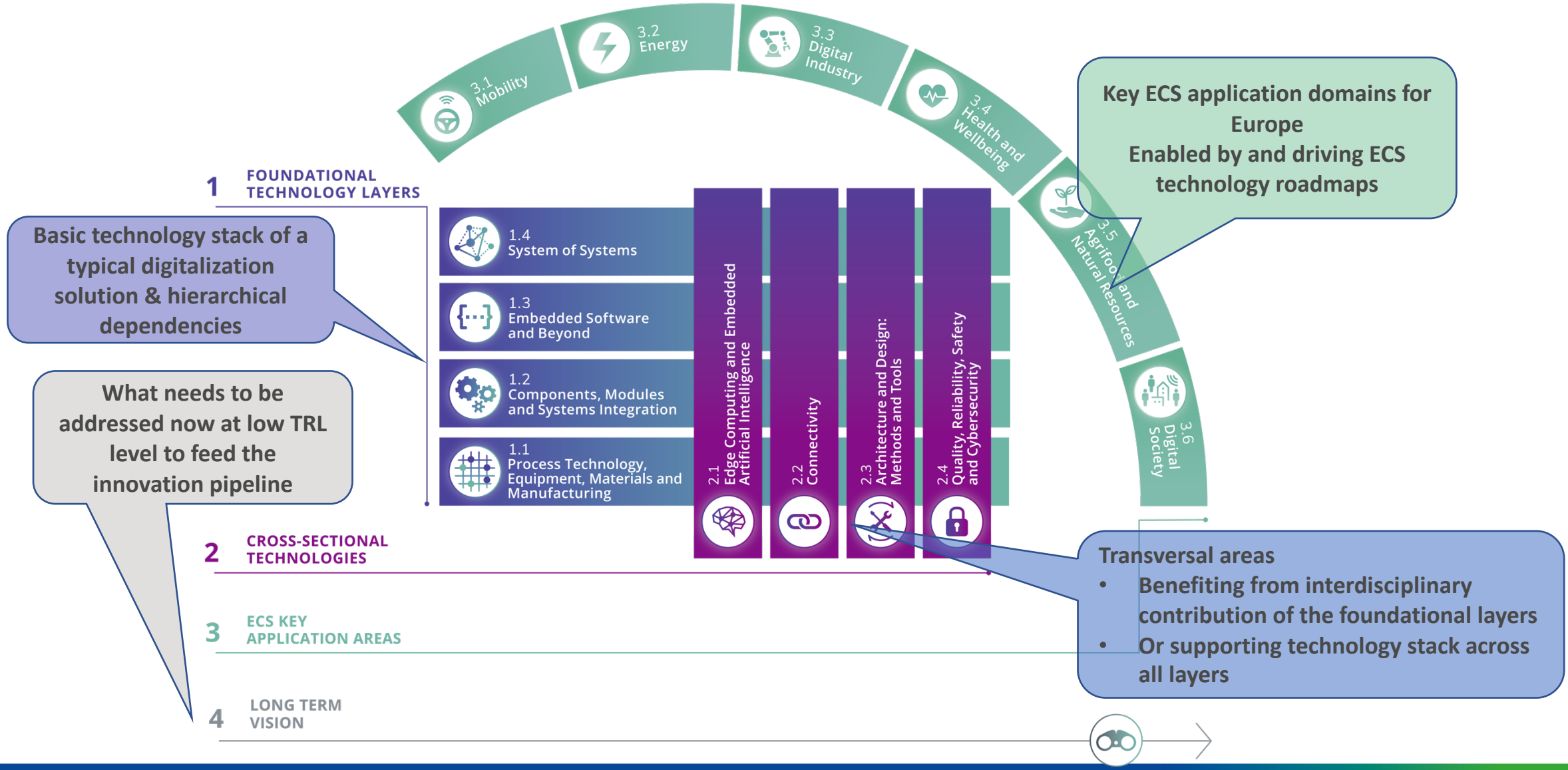
EUCloudEdgeIoT.eu

Open Continuum

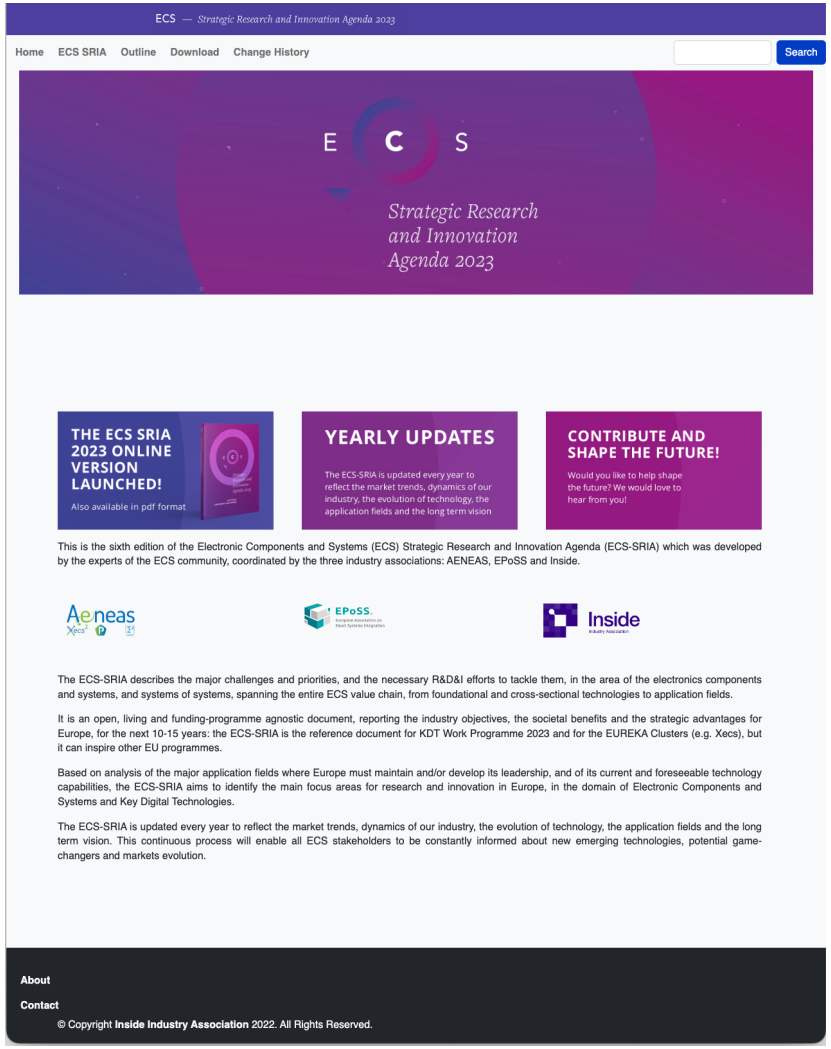
CCAM
CONNECTED, COOPERATIVE & AUTOMATED MOBILITY

And many others…

ECS-SRIA structure

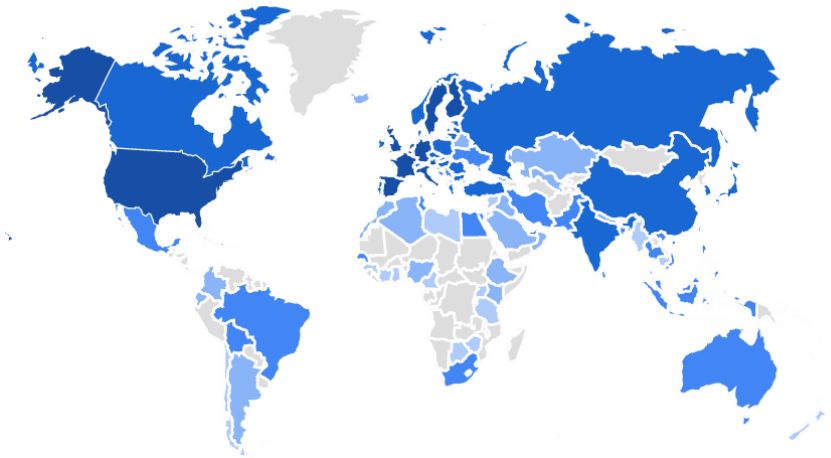


ECS-SRIA Web Site



- ECS-SRIA 2024 published on the 06/02/2024
- Web version only: https://ecssria.eu/
- Increased visibility and accessibility
- Simple to browse with hyperlinks
- Attract new talents and experts
- Native indexing and analytics
- More advanced functionalities for:
  - Topics search
  - Selective reading
- W3C standard

Users by Country in the last 12 Months



COUNTRY	USERS
Netherlands	1.3K
France	1.2K
Finland	1K
United States	1K
Germany	976
Austria	724
Spain	467

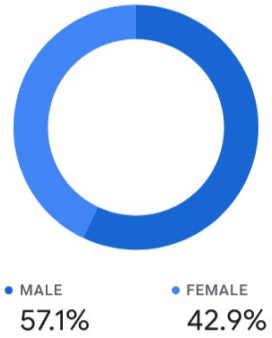
1	Netherlands	1,257
2	France	1,157
3	Finland	1,005
4	United States	1,004
5	Germany	976
6	Austria	724
7	Spain	467
8	Italy	430
9	Belgium	380
10	Sweden	373
11	United Kingdom	315
12	Türkiye	270
13	China	148
14	Portugal	136
15	Greece	126
16	Ireland	125
17	Norway	116
18	Switzerland	112
19	Japan	110
20	India	95

21	Poland	90
22	Canada	80
23	South Korea	66
24	Denmark	63
25	Luxembourg	52
26	Taiwan	52
27	Czechia	45
28	Singapore	38
29	Romania	36
30	Israel	35
31	Latvia	34
32	Hungary	32
33	Slovenia	32
34	Estonia	22
35	Hong Kong	22
36	Lithuania	22
37	Russia	22
38	United Arab Emirates	20
39	Bulgaria	19
40	Ukraine	16

Visited from a total of 110 countries

Accesses and user number (last 12 months)

ECS-SRIA PAGE, PART, CHAPTER	Accesses	Users
About	**8111**	**4514**
Introduction and overview	**8604**	**4621**
ECS SRIA outline	**1610**	**917**
1. Foundational Technology Layers (total for part 1)	**8019**	**2355**
1.1 Process Technology, Equipment, Materials And Manufacturing	3426	671
1.2 Components, Modules and Systems Integration	2070	709
1.3 Embedded Software and Beyond	1480	538
1.4 System of Systems	1043	437
2. Cross-Sectional Technologies (total for part 2)	**6165**	**2407**
2.1 Edge computing and embedded Artificial Intelligence	2576	986
2.2 Connectivity	1220	354
2.3 Architecture and Design: Method And Tools	1439	710
2.4 Quality, Reliability, Safety And Cybersecurity	930	357
3. ECS Key Application Areas (total for part 3)	**6092**	**2239**
3.1 Mobility	1429	487
3.2 Energy	884	333
3.3 Digital Industry	1066	384
3.4 Health & Wellbeing	1139	452
3.5 Agrifood And Natural Resources	842	271
3.6 Digital Society	732	312
4. Long-Term Vision	**872**	**398**



The number of accesses and users is equally distributed across the the main parts

Total number of visits to the entire website: 48120

Main interests of users according to Google Analytics:

1. Technology (54% of the users)
2. Economy (40% of the users)
3. Business (37% of the users)
4. Politics (33% of the users)

ECS SRIA 2024 Edition
What’s new ?

Link with Pilot Lines and the Design Platform

- Principles
  - SRIA is the industry expression of its R&I plans, and is funding instrument agnostic
  - The SRIA will not address how Pilot Lines and the Design Platform must be run
  - It can however identify research topics of interest for the industry where Pilot Lines and the Design Platforms can help
  - This will feed the research roadmaps of these mechanisms
- Main SRIA updates
  - New chapter 0 (Introduction) section
  - Updated Chapter 2.3 (Architecture and Design – Methods and Tools)

New Chapter 0 Section "Make it happen"

- Rationale for addressing the design platform and pilot lines within the ECS SRIA
- Table linking SRIA chapters and those instruments
  - Pilot lines being considered : The three most likely to be launched in a first batch (as of the time of finalising the SRIA 2024 edition)
  - Additional column for other pilot lines
  - Partial view :

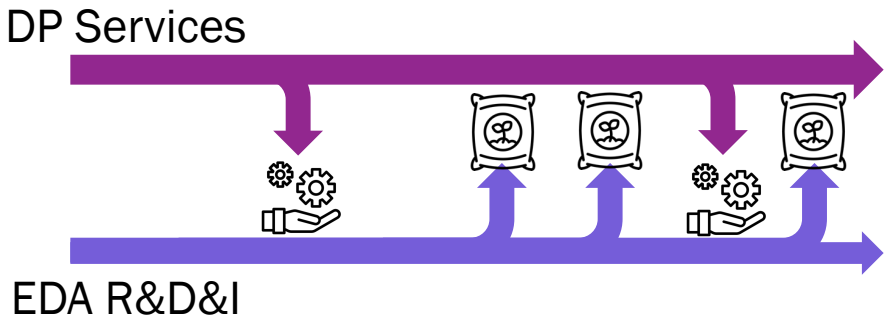
	Design platform	Advanced 2nm and beyond	FD-SOI	Advanced Packaging and Heterogeneous Integration	Other pilot lines
1.1 Process Technology, Equipment, Materials and Manufacturing		Launching ground for new processes, equipment technologies and materials	Low-power consumption, radiation hardness, More than Moore app.	Introduce materials and process innovations as well as advanced manufacturing, test and inspection equipment for future AP/HI systems.	
1.2 Components, Modules and Systems Integration	Improve design capabilites to become a closed loop (i.e., to include feedbacks from the production process and from the field use, respectively) as well as define the new sets of interfaces for the complex integration solutions at die / module / system levels as needed for implementing heterogeneous and chiplet approaches - in particular for ECS applications that will be exposed to demanding and harsh environments (as these ECS are essential for our European backbone industry -automotive, energy, industry, health, ...- and not sufficiently and securely addressed by the worldwide leading players).	Impact of advanced node inflections like backside power distribution networks, forksheet, CFET and 2D material channels 3D heterogeneous integration in chiplet implementation		Enable enhanced and diversified functionalities (e.g. combined sensing, processing, communication, ...) in small form factor electronic components and systems.	Platforms leading to the scalability of elements enabling connection between the digital and physical worlds (e.g. MEMS, integrated photonics, power electronics, quantum approaches...) in silicon or silicon alternative technologies will provide, together with logical circuitry, additional essential building blocks to be integrated in full fledged electronic systems
1.3 Embedded software and Beyond		Design Technology Co-Optimisation	Design Technology Co-Optimisation		

- Specific expectations vs. the design platform

Updated Chapter 2.3
Adds-on regarding Design Platform

New

- Strategic advantage for the EU
  - DP expected to support technical enhancements and facilitate the development of ecosystems
- For each Major Challenge, addition of two aspects
  - R&I focus areas which could be supported by the design platform
  - Research feeding design platform evolution



Artificial Intelligence

- ECS as an enabler of AI
  - Meeting performance needs
  - New concepts and architectures mitigating AI-related energy consumption
    - Moving towards AI at the edge
    - In-memory computing
- AI as an enabler of ECS
  - AI-based methods for ECS architecture exploration and optimization
  - AI-based guidance in the V&V process
  - Automatic generation of test cases
- AI support to manage AI-induced complexity
- Trustable, responsible AI-based ECS

Quantum Technologies

- Joint workshops organized in 2023 between ECS SRIA chapter leaders and QuIC Working Group leaders
  - QuIC: European Quantum Industry Consortium
- Developments in several chapters on
  - Quantum sensing
  - Quantum computing
  - Quantum cryptography
  - Enabling ECS technologies

Sustainability

Enriched

- Can be found under many SRIA Chapters
  - Specific additions this year in chapters 1.2 and Long Term Vision
- Eco-Design of ECS to promote circularity
  - Set up repair process
- Sustainable manufacturing of ECS
  - Zero waste
  - Natural resource consumption reduction & reuse (power, water)
  - Reduce CO_2 and Green House Gas emissions
  - Handling the PFAS challenge
  - Critical raw materials use
- Sustainable products and business models
  - Repair index
  - Product categories
  - Repair as business

… and many other updates

- Tighter integration with RISC-V and Open Source HW
- Lidar, radar and camera integration
- Photonics integration
- Hardware virtualisation for efficient software engineering
- New frequency bands for 6G
- EDA research topics
- SoC for mobility
- Software-defined vehicle
- Revisiting the European health ecosystem
- Agriculture decarbonisation

ECS SRIA 2024 Edition
Short demo

https://ecssria.eu/

ECS SRIA 2025

The 2024 SRIA is completed… Long live the 2025 edition !

Patrick Cogez
AENEAS
Chairman

Paolo Azzoni
Inside IA
Co-chairman

Matthias Küntzel
EPoSS
Co-chairman

- Kick-off meeting 21/02/2024 (with chapter leaders)
- Aiming at conciseness… while still meeting the needs of the technical community
- Target delivery date – October 2024
  - For adoption by GB in November meeting
- Dedicated group focused on a new “synopsis” document

Welcome !

Final words

- The ECS SRIA covers the R&I needs identified by the ECS industry
- It plays a major role in aligning R&I priorities within the ECS community with funding instruments
- It is a coordination and knowledge exchange instrument with other communities
- Moving to the Chips Act increases its relevance
- You can (and should) be part of it !

THANK YOU !

ECS

Strategic Research and Innovation Agenda 2024

Aeneas

EPoSS. European Association on Smart Systems Integration

Inside Industry Association